CLAIMS

What is claimed is:

1. A transistor comprising:

a channel region;

a first gate on top of said channel region;

a second gate below said channel region;

wherein said first gate and said second gate are electrically separated from each other.

2. The transistor of claim 1, wherein said first gate comprises a different doping concentration that said second gate.

3. The transistor of claim 1, wherein said first gate comprises a different doping species than said second gate.

4. The transistor of claim 1, further comprising a first gate dielectric below said first gate and a second gate dielectric above said second gate.

5. The transistor of claim 1, wherein said first gate has a first conductive contact and said second gate has a second conductive contact and said first conductive contact and said second conductive contact are coplanar.

6. The transistor of claim 1, wherein said first gate comprises a different material than said second gate.

7. The transistor of claim 1, wherein said first gate comprises a different thickness than said second gate.

8. The transistor of claim 1, wherein said first gate, said second gate and said channel region form a planarized structure.

9. The transistor of claim 4, wherein said first gate dielectric comprises a different material than said second gate dielectric.

10. The transistor of claim 4, wherein said first gate dielectric comprises a different thickness than said second gate dielectric.

11. A semiconductor chip having at least one transistor, said transistor comprising:

a channel region;

a first gate on top of said channel region;

a second gate below said channel region;

wherein said first gate comprises a different material than said second gate.

12. The semiconductor chip of claim 11, wherein said first gate and said second gate have

different dopant concentrations.

13. The semiconductor chip of claim 11, wherein said first gate and said second gate have different dopant species.

14. The semiconductor chip of claim 11, further comprising a first gate dielectric below said first gate and a second gate dielectric above said second gate.

15. The semiconductor chip of claim 14, wherein said first gate dielectric comprises a different material than said second gate dielectric.

16. The semiconductor chip of claim 14, wherein said first gate dielectric comprises a different thickness than said second gate dielectric.

17. The semiconductor chip of claim 11, wherein said first gate has a first conductive contact and said second gate has a second conductive contact and said first conductive contact and said second conductive contact are coplanar.

18. The semiconductor chip of claim 11, wherein said first gate and said second gate are electrically separated.

19. The semiconductor chip of claim 11, wherein said first gate and said second gate have

different thicknesses.

20. The semiconductor chip of claim 11, wherein said first gate, said second gate and said channel region form a planarized structure.

21. A method of forming a transistor comprising:

forming a laminate structure including a first gate over a channel region;

removing portions of said laminate below said channel region; and,

forming a second gate below said channel region,

wherein said first gate and said second gate are electrically separated from each other.

22. The method of forming a transistor according to claim 21, wherein said first gate supports said channel region during said removing process.

23. The method of forming a transistor according to claim 21, wherein said first gate comprises a different doping concentration than said second gate.

24. The method of forming a transistor according to claim 21, further comprising applying different doping species to said first gate and said second gate.

25. The method of forming a transistor according to claim 21, further comprising forming a first gate dielectric below said first gate and a second gate dielectric above said second gate.

26. The method of forming a transistor according to claim 24, wherein said first gate dielectric comprises a different material than said second gate dielectric.

27. The method of forming a transistor according to claim 24, wherein said first gate dielectric comprises a different thickness than said second gate dielectric.

28. The method of forming a transistor according to claim 21, further comprising forming a first gate oxide below said first gate and a second gate oxide above said second gate.

29. The method of forming a transistor according to claim 21, wherein said first gate has a first conductive contact and said second gate has a second conductive contact and said first conductive contact and said second conductive contact are coplanar.

30. The method of forming a transistor according to claim 21, wherein said first gate comprises a different material than said second gate.

31. The method of forming a transistor according to claim 21, wherein said first gate comprises a different thickness than said second gate.

32. The method of forming a transistor according to claim 21, wherein said first gate, said second gate and said channel region form a planarized structure.

33. A method of manufacturing a double-gate transistor comprising:

forming a laminated structure having a channel layer and first insulating layers on each side of said channel layer;

forming openings in said laminated structure;

forming drain and source regions in said openings;

removing portions of said laminated structure to leave a first portion of said channel layer exposed;

forming a first gate dielectric on said channel layer;

forming a first gate electrode on said first gate dielectric layer;

removing portions of said laminated structure to leave a second portion of said channel layer exposed;

forming a second gate dielectric layer on said channel layer;

forming a second gate electrode on said second gate dielectric layer;

doping said drain and source regions,

wherein said first gate electrode and said second gate electrode are formed independently of each other.

34. The method in claim 33, wherein, said first and second gate electrode are electrically separated.

35. The method in claim 33, wherein said doping of said drain and source regions comprises

a self-aligned ion implantation.

36. The method in claim 33, wherein said method further comprises forming said first gate electrode to have a thickness and greater than that of said second gate electrode.

37. The method in claim 33, wherein said method further comprises forming said first gate to have a width greater than that of said second gate.

38. The method in claim 33, wherein said method further comprises forming said first gate dielectric to have a width greater than that of said second gate dielectric.

39. The method in claim 33, further comprising forming said first gate from a first material and said second gate from a second material.

40. The method in claim 33, further comprising forming said first gate dielectric from a first material and said second gate dielectric from a second material.

41. The method in claim 33, wherein said removing portions of said laminate structure leaves a second portion of said channel layer exposed, forms a tunnel in said laminate, and,

wherein said tunnel is formed between an upper layer and a lower layer and said lower layer.

42. The method in claim 33, wherein said first gate dielectric comprises a different material than said second gate dielectric.

43. The method of forming a transistor according to claim 33, wherein said first gate dielectric has a different thickness than said second gate dielectric.